IOSR Journal of Electronics and Communication Engineering (IOSR-JECE)
e-ISSN: 2278-2834, p-ISSN: 2278-8735
PP 31-37
www.iosrjournals.org

Review of Reversible Synchronous Sequential Circuits

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Abstract: *In early 70`s one computer requires one whole room and now a days we kept commuter in our pockets, how it`s happens? This happens because we did tremendous revaluation in VLSI field. We rapidly decrease size of transistors. After decades of continuous improvements and shrinking feature sizes, the development of conventional computing technologies faces massive challenges. In particular, power dissipation in today's computer chips becomes critical. Reversible computation is a best alternative to these technologies, where we want to reduced or even eliminatedpower dissipation. Reversible logic has become very capable for low power design using emerging computing technologies. A number of good works have been reported on reversible combinational circuit design. However, a small number of works reported on the design of reversible latches and flip-flops on the top of reversible combinational gates and suggested that sequential circuits be built by replacing the latches and flip-flops and associated combinational gates of the traditional irreversible designs by their reversible counter parts. This replacement technique is not very promising, because it leads to high quantum cost and garbage outputs.*

Keywords*–garbage input, quantum cost, reversible gate*

I. Introduction

Power dissipation is one of the crucial issues in today's technology. The cause of power dissipation is loss of information and this firstly predicted by R. Landaure in 1960. According to his principal k*T*ln2 joules energy dissipate into environment when we loss one bit of information, where k is the Boltzmann's constant and k=1.38x10 -23 J/K, T is the absolute temperature in Kelvin.[1] Moore`s law said that after 18 month's transistor density on chip get doubles , if we continued with this till 2020 then it is impossible to remove heat dissipation [2] . One more researcher Bennett in 1973 showed that using thermodynamics principal, if we use loss lesstechnology then we can reduces or eliminates power dissipation [3]. This information loss less technology is only built by reversible circuit.De Benedici [4] shows that, for power consumption reasons, reversible circuits will be the only technology possible to build supercomputers of the future. Therefore, reversibility will become an essential property in future logic circuit design and synthesis algorithms. Reversible circuits have been implemented in ultra-low-power CMOS technology[5], optical technology[6], quantum technology, nanotechnology[7], quantum dot[8], and DNA technology[9].

Most of the researcher`s work in reversible logic is only in combinational logic synthesis. Only limited attempts have been made in the field of reversible sequential circuits. Some researchers argue that we cannot implement sequential circuits in reversible logic because there is no provision for feedback loop. However, in 1980, Toffoli [10] argued that if the feedback is provided through a delay element, thenThe feedback information will be available as the input to the reversible combinational circuit in the next clock cycle and sequential logic is possible.There are mainly two ways for implementations of reversible sequential circuits using replacement technique[11]–[14] and direct design using reversible gates. All the flip flops and latches in this paper are compared with respective quantum cost and garbage inputs.

II. Level Triggered Flip Flop Using Reversible Logic

1.1 RS Latch

In [14] there are two ways to design RS latch, using Toffoli gate and using Fredkin gate as shown in below figures. This RS latch has quantum cost 18 and garbage inputs are 3.

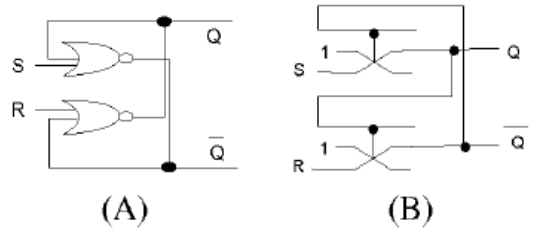


Fig 1: RS latch built from (A) Conventional Gates (B) Fredkin Gates

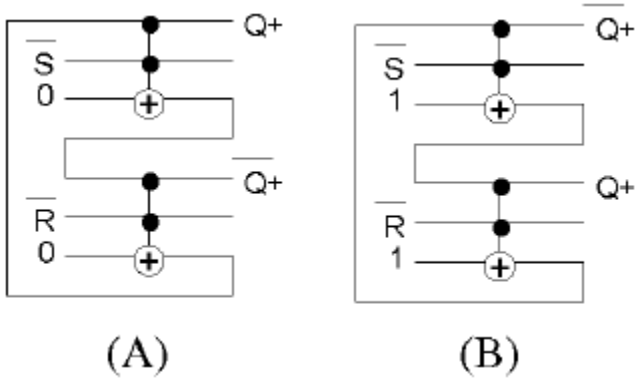


Fig 1: RS latch built from two Toffoli Gates

1. JK Flip Flop

In [12] positive edge trigger JK flip flop is designed using four Fredkin gates as shown in below figure. Quantum cost of this flip flop is 12 and it has 4 garbage inputs.

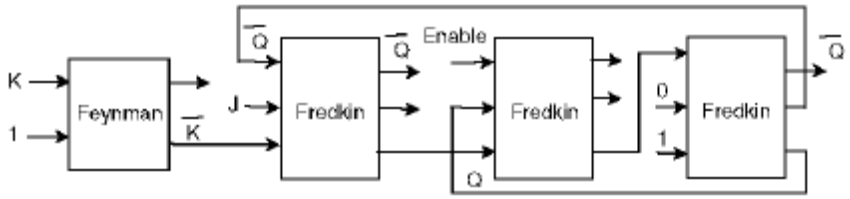


Fig 2: Positive edge triggered JK Flip Flop in [12]

In [14] JK flip flop is designed usingFredkin gate and FG gate. It has quantum cost 12 and 3 garbage inputs. It has much lesser quantum cost as compare to [12].

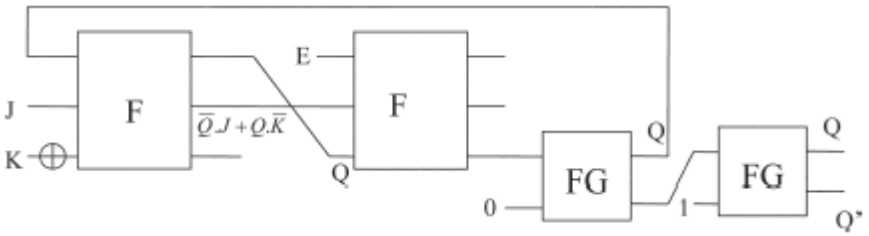
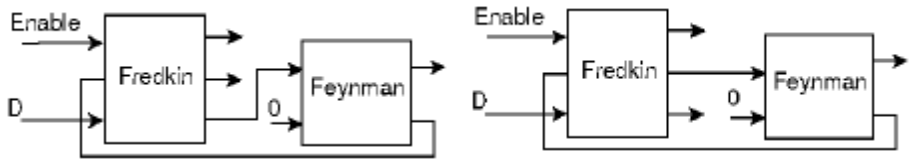


Fig 3: JK Flip Flop in [14]

2. D Flip Flop

In [12] positive leveltriggered D flips flop is designed using single Feynman and single Fredkingate, Where Fredkin gate is used as a 2:1 mux and Feynman gate is used for fan-out . In [12] they designed both positive level and negative leveltriggered D flip flops and they are represented in following figures. This D flip flop has quantum cost 10 and garbage input 2.



(A) (B)

Fig 4: D flip flop for (A) Positive level triggered (B) Negative level triggered

In [13] D flip flop is designed to avoid fan-out problem which occurs in [13].It`s implementation is shown in below figure. This design has 6 quantum cost and 2 garbage inputs.

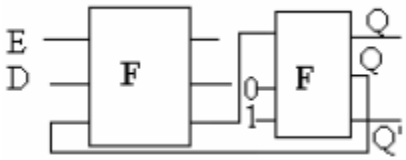


Fig 5: D flip flop in [13] to avoid fan-out problem.

The design in [14] used two Feynman gates and one Fredkin gate it's diagram is shown below. It has 7 quantum cost and 2 garbage inputs.

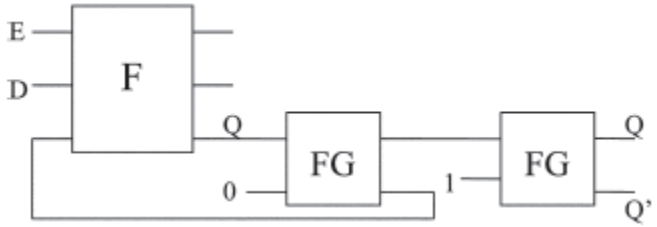


Fig 6: D flip flop in [14]

The design in [13] has less quantum cost and garbage input as compare to design with [11] and [14].

3. T Flip Flop

In [12] Positive level triggered flip flop is designed by using two Feynman and one Fredkin gate. It requires 7 quantum cost and 2 garbage inputs.

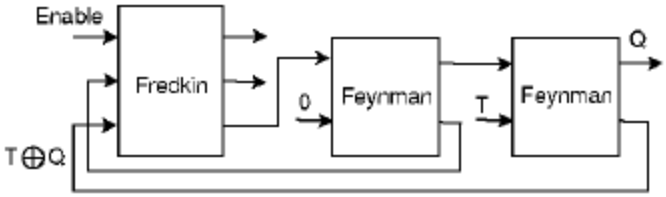


Fig 7: T Flip Flop in [12]

In [13] T triggered flip flop is designed by using one Fredkin gate and Toffoli gate. It has 6 quantum cost and 2 garbage inputs.

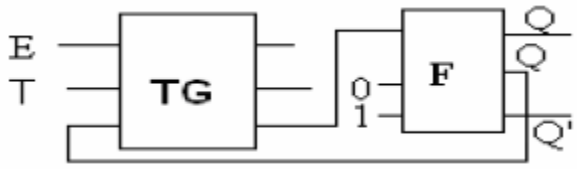


Fig 7: T Flip Flop in [13]

In [14] T flip flop is designed by using one Peres gate and Feynman gate. It has 6 quantum cost and 2 garbage inputs.

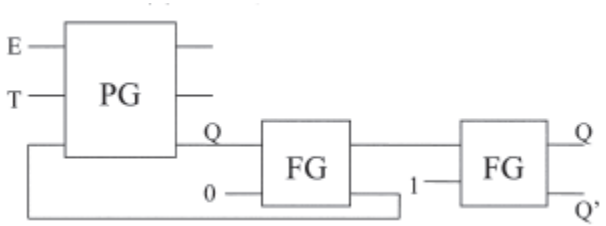


Fig 7: T Flip Flop in [14]

III. Master Slave Flip Flops In Reversible Logic

1. RS flip flop

Master slave RS Flip flop in [11] is given below. It has 50 quantum cost and 16 garbage inputs.

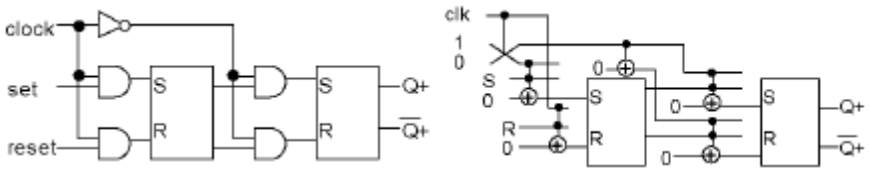


Fig 8: Master Slave RS flip flop in [11]

Master slave RS flip flop in [14] is given below, to implement this flip flop we requires one Fredkin gate, four Feynman gate and one Toffoli gate. It has 24 quantum cost and 3

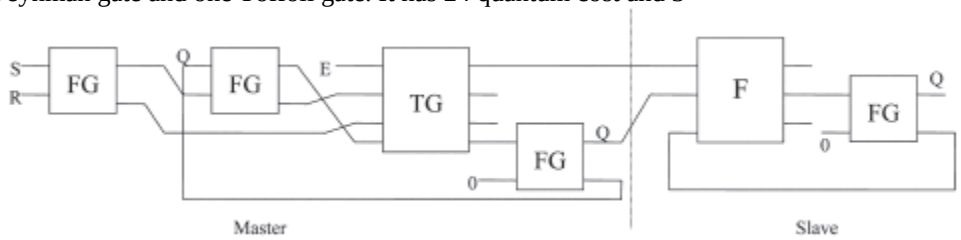
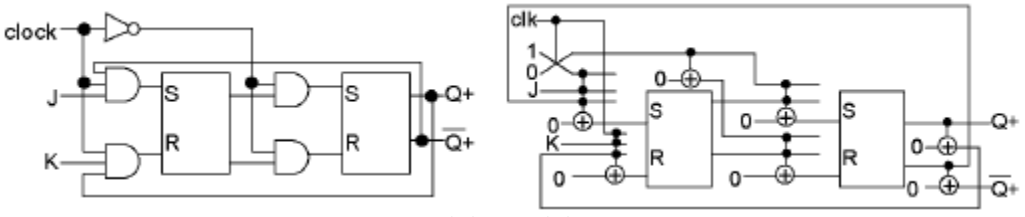


Fig 9: Master Slave RS flip flop in [14]

2. JK flip flop

Following figure shows JK flip flop in [11].It has 62 quantum cost and 18 garbage inputs



(A) (B)

Fig 9: Master Slave JK flip flop in [29]

In [12] JK flip flop is designed by using two Fredkin gate and two Feynman gate. It has 22 quantum cost and 6 garbage inputs

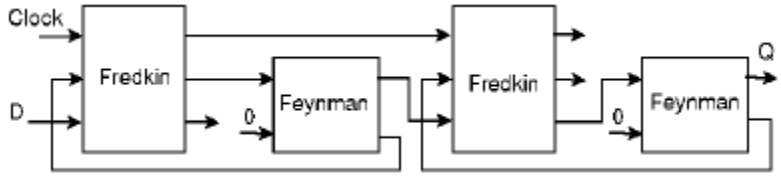


Fig 10: Master Slave JK flip flop in [12]

In [14] JK flip flop is designed by using three Fredkin gate and two Feynman gate. It has 18 quantum cost and 3 garbage inputs.

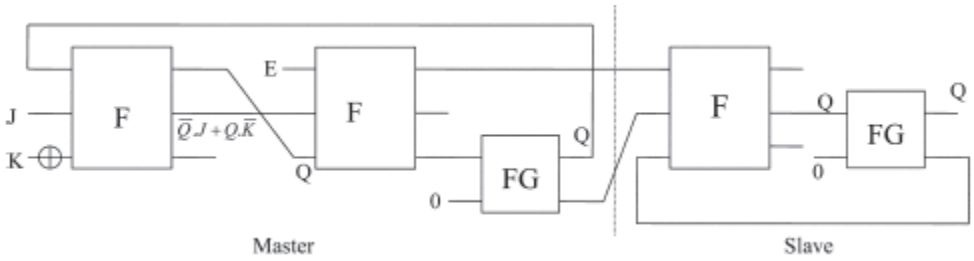
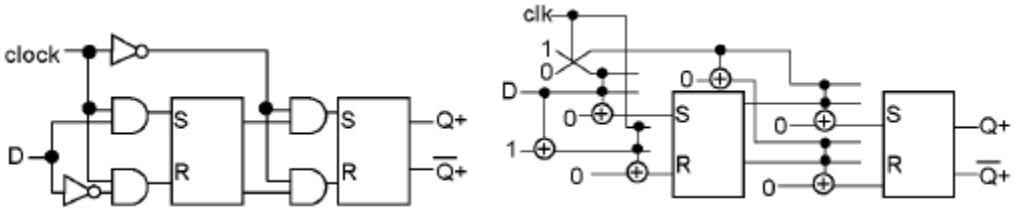


Fig 11: Master Slave JK flip flop in [14]

Out of these three JK flip flop`s [14] flip flop is best because it has lowest quantum cost and garbage inputs.

3. D flip flop

D flip flop in [11] is given below it has 51 quantum cost and 16 garbage inputs



(A) (B)

Fig 12: Master Slave D flip flop in [11]

In [12] D flip flop is design in following way for that it requires two Feynman and two Fredkin gates. It`s quantum cost is 22 and garbage input is 6.

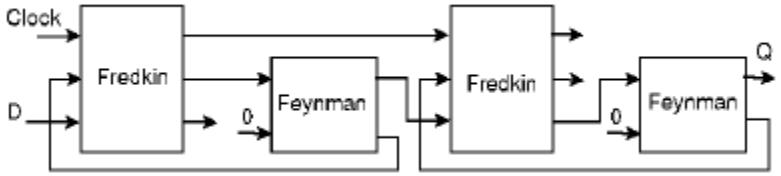


Fig 12: Master Slave D flip flop in [12]

In [13] D flip flop is design by usingthree Feynman and two Fredkin gates. It`s quantum cost is 13 and garbage input is 4.

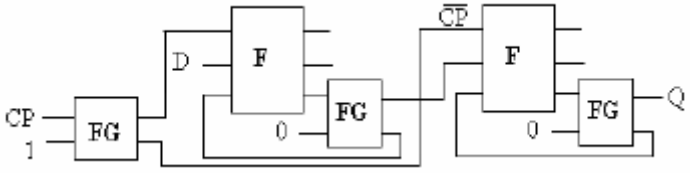


Fig 13: Master Slave D flip flop in [13]

Below figure shows the master slave D flip flop in [14]. It`s quantum cost is 13 and garbage input is 2.

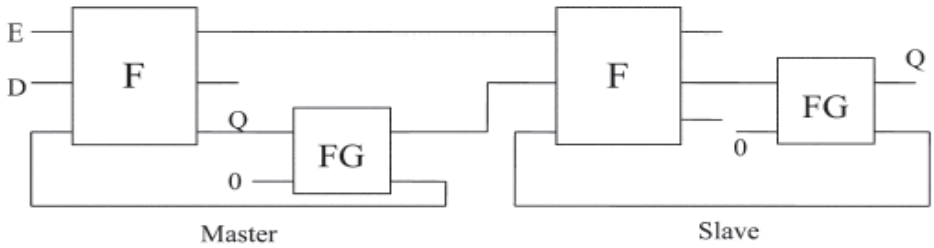


Fig 14: Master Slave D flip flop in [14]

4. T flip flop

Master Slave T flip flop in [11] is shown below. It`s quantum cost is 63 and garbage input is 18.

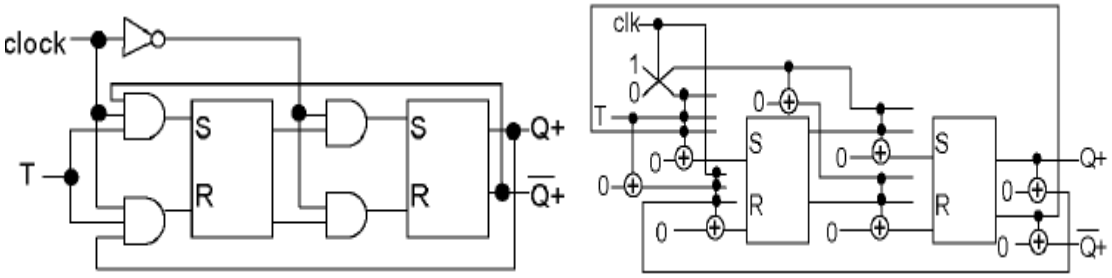


Fig 15: Master Slave T flip flop in [11]

Master Slave T flip flop in [12] is shown below. It`s quantum cost is 13 and garbage input is 3.

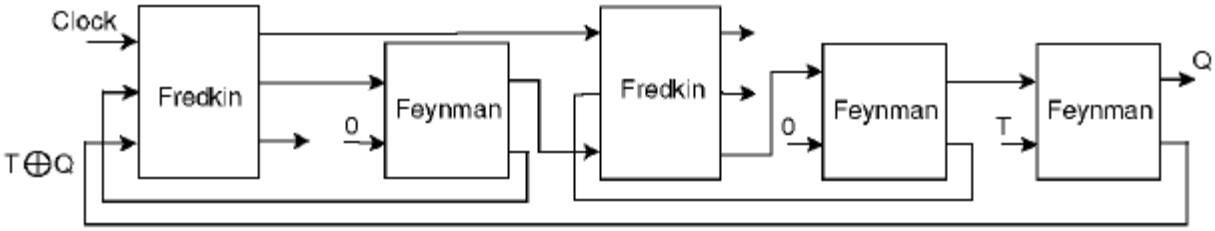


Fig 15: Master Slave T flip flop in [12]

Master Slave T flip flop in [13] is shown below. It`s quantum cost is 17 and garbage input is 4.

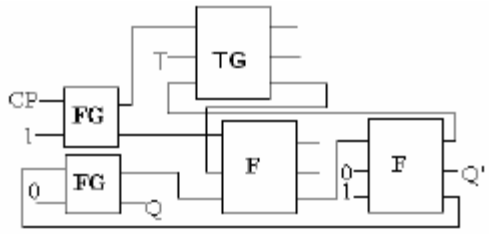


Fig 16: Master Slave T flip flop in [13]

Master Slave T flip flop in [14] is shown below. It`s quantum cost is 12 and garbage input is 2.

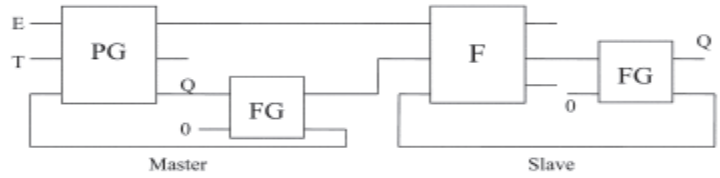


Fig 17: Master Slave T flip flop in [14]

Following Table compares' all the flip flops. This comparison is based on quantum cost and garbage output and they are separated by comma.

Table 1: Comparison of realization costs and number of garbage outputs (separated by comma) of level-triggered flip-flop and edge-triggered/master-slave flip-flop designs

Ref.	**Level-triggered flip-flop**				**Master-Slave flip-flop**			
[11]								
[12]								
[13]								
[14]								

IV. Conclusion

Reversible logic has shown a good promise for low-power design using emerging computing technologies. A good number of design methods for reversible combinational circuits have been proposed [13]–[22]. However, only a very limited works have been reported on reversible sequential circuit design [11]–[30]. In this paper we give review of the entire level triggered and master slave flip flop from four different papers. This review is concentrated on quantum cost and garbage inputs. All the flip flop are summarized in table 1 and best are shown in bold.

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